Exhibit 26

Robert George · 3rd

Senior Fellow, Lead SoC Architect/Product Architect Radeon Technology Group (RTG) at AMD

- AMD
- Naval Postgraduate School

Austin, Texas, United States · **Contact info**

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About

Seasoned computer architect with more than 30 years' experience and demonstrated successes in the architecture, micro-architecture, design and development of high-performance microprocessor, graphics and SoC architectures.

Driving corporate-level technology direction, and leading architecture teams to define and optimize new products for performance, power, schedule and cost.

More recently, driving radical SoC/product modularity improvements via 3D chip architectures, chiplets and advanced 3D packaging, UCIE.

A core member of the architecture team that defined the Intel virtualization extensions on Prescott and Tejas, and the Intel Common System Interconnect (iTanium coherency) fabric.

Chief architect and technical lead at AMD for the PlayStation 4, PS4 Pro, and

PlayStation 5.

Specialties

• Rare combination of CPU and GPU micro-architecture expertise, including CPU/GPU inter-operation, internal/distributed cache coherency, coherent interconnects ….

• Super-scalar and OOO CPU architecture, graphics/GPU architecture, chip multiprocessing/many-core arrays, heterogeneous CMP and co-processor architectures, fine-grained threading and vector processing.

• Memory coherency protocols, hardware synchronization mechanisms, interconnection networks.

• Virtual Machine architectures

• Data integrity architecture and soft error analysis

• Identifying and analyzing long-term technology trends and competitive analysis.

• Working with customers/OEMs and the corresponding corporate business units to develop, scope, rank, and prioritize product requirements, use cases.

Activity

508 followers

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Experience

AMD

10 yrs 2 mos

Senior Fellow, SoC Architecture Lead, Radeon Technology Group (RTG)

Full-time

Jul 2016 - Present · 6 yrs 9 mos

Chief Architect for Radeon System on Chip/discrete GPU architectures

• Leading a team of architects defining and architecting a roadmap of next generation GPU products: 6 products spread across 2 architecture generations, and 3 process technologies, including discrete GPU

generations, and 5 process technologies, including discrete GPU, datacenter/machine learning, and low power/mobility products.

• Driving a broad collaboration with IP leads across the company, process and power teams and business leads to architect Radeon dGPU products precisely aligned against the competition and optimized for Performance/mm2, Performance/Watt, Performance/Bandwidth

• Leveraging next-generation technologies including cutting-edge 3D packaging and chiplet construction, stacked caches, large memory caches, HBM and GDDR-6 memory

Fellow, Consoles/Semi-custom Business Unit

Feb 2013 - Jul 2016 · 3 yrs 6 mos
Austin, Texas Area

Chief architect and technical lead at AMD for the PlayStation 4, PS4 Pro, PlayStation 5 APU (CPU + GPU).

• Worked closely with Sony to define, architect, and champion a series of next generation APU's

Principal Architect

NVIDIA
Jul 2008 - Feb 2013 · 4 yrs 8 mos

2011 - 2013
...
...see more

Senior Staff Architect

Intel Corp
1998 - 2008 · 10 yrs

Led the Tejas VT Virtual Machine architecture definition

Education

Naval Postgraduate School

Master of Science (M.S.), Computer Engineering
1994 - 1995

Virginia Tech

Bachelor of Science (B.S.), Computer Engineering
1984 - 1988

Skills

Computer Architecture


Endorsed by Anirudh Acharya and 2 others who are highly skilled at this


Endorsed by 4 colleagues at AMD

18 endorsements

Microprocessors


Endorsed by Fred Gruner who is highly skilled at this


Endorsed by 3 colleagues at AMD

14 endorsements

Microarchitecture


Endorsed by 3 colleagues at AMD

11 endorsements

Show all 10 skills →

Publications

Intel 870: a building block for cost-effective, scalable servers

IEEE · Mar 1, 2002

Show publication

A rate-monotonic scheduler for the real-time control of autonomous robots

Proceedings of IEEE International Conference on Robotics and Automation · Apr 1, 1996

Show publication

Patents

Method and apparatus for the synchronization of distributed caches

US 8,046,539 · Issued Jun 5, 2009

See patent

The present invention to cache memory systems and more particularly to a hierarchical caching protocol suitable for use with distributed caches.

Maintaining processor resources during architectural events

US 7,562,179 · Issued Jul 30, 2004

See patent

The first of many Vanderpool Technology (Processor Virtualization) patents.

Associating address space identifiers with active contexts

US 7,552,254 · Issued Jul 30, 2003

See patent

Cache-coherent TLB's for synchronizing page tables between multiprocessors, especially big and little (co-processor) cores.

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Interests

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